

Experimental demonstration of plasmon–plasmon scattering paves the way for electromagnetic wave-based digital logic concept

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ABSTRACT

We report the experimental demonstration of plasmon–plasmon scattering at room temperature in the inversion layer of a patterned metal–oxide–semiconductor structure. This fundamental result paves the way for the development of plasmon–plasmon scattering logic, a revolutionary digital logic concept based on the generation, propagation, and manipulation of plasmons in an electron fluid, which was previously theoretically projected to exhibit femtojoule power dissipations and femtosecond switching speeds, while not demanding expensive nanometer-scale silicon (Si) technology fabrication processes for its implementation.

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Downscaling, the relentless size reduction approach to enhance the performance of field-effect transistors (FETs), has fueled the phenomenal progress in computing integrated circuit (IC) technology (Moore's law) for the past 50 years.^{1–9} However, the physical device limitations concomitant with extreme downscaling and its prohibitive fabrication cost are great obstacles ushering the demise of such a paradigm.^{9–11} Due to the urgent need¹¹ of overcoming the diminishing returns and cost of continuing device downscaling, many “beyond CMOS” devices are being pursued, which exploit various physical phenomena, such as^{9,12} (1) particle (electron/hole) charge manipulation (e.g., the Tunneling FET (TFET), the graphene PN junction, and the bilayer pseudo-spin-FET); (2) electron spin manipulation (e.g., the spinFET); (3) magnetic domain wall manipulation (e.g., the spin transfer torque/domain wall device); (4) spin wave manipulation (e.g., the spin wave device); and (5) magnetic coupling manipulation (e.g., nanomagnetic logic and probabilistic spin logic). Many of these device approaches, however, are

not amenable to implementation in the established CMOS fabrication infrastructure and, requiring fabrication process modifications, in particular, incorporation of III–V compound semiconductors, graphene, or ferromagnetic or magnetic materials, remain under open-ended development.

While the operation of plasmon–plasmon scattering logic (PPL)^{13,14} exploits the biasing of a patterned Metal–Oxide–Semiconductor (MOS) structure into, for example, inversion, similarly to FETs,¹⁵ the similarity stops there; to facilitate its understanding, we present it in three steps. First, we have the MOS structure in Figs. 1(a) and 1(b).¹⁵ Once V_{Bias} sets the OS interface into inversion and, thus, creates a static electron charge density layer there, a quasi-transverse electromagnetic wave (q-TEM) S_{Bias} locally disturbs the electron density at the point of impinging into a purposely chosen long (many micrometers) channel. Due to the long channel, on its own, the charge disturbance would subside in a charge density fluctuation relaxation time; thus, we deemed it to

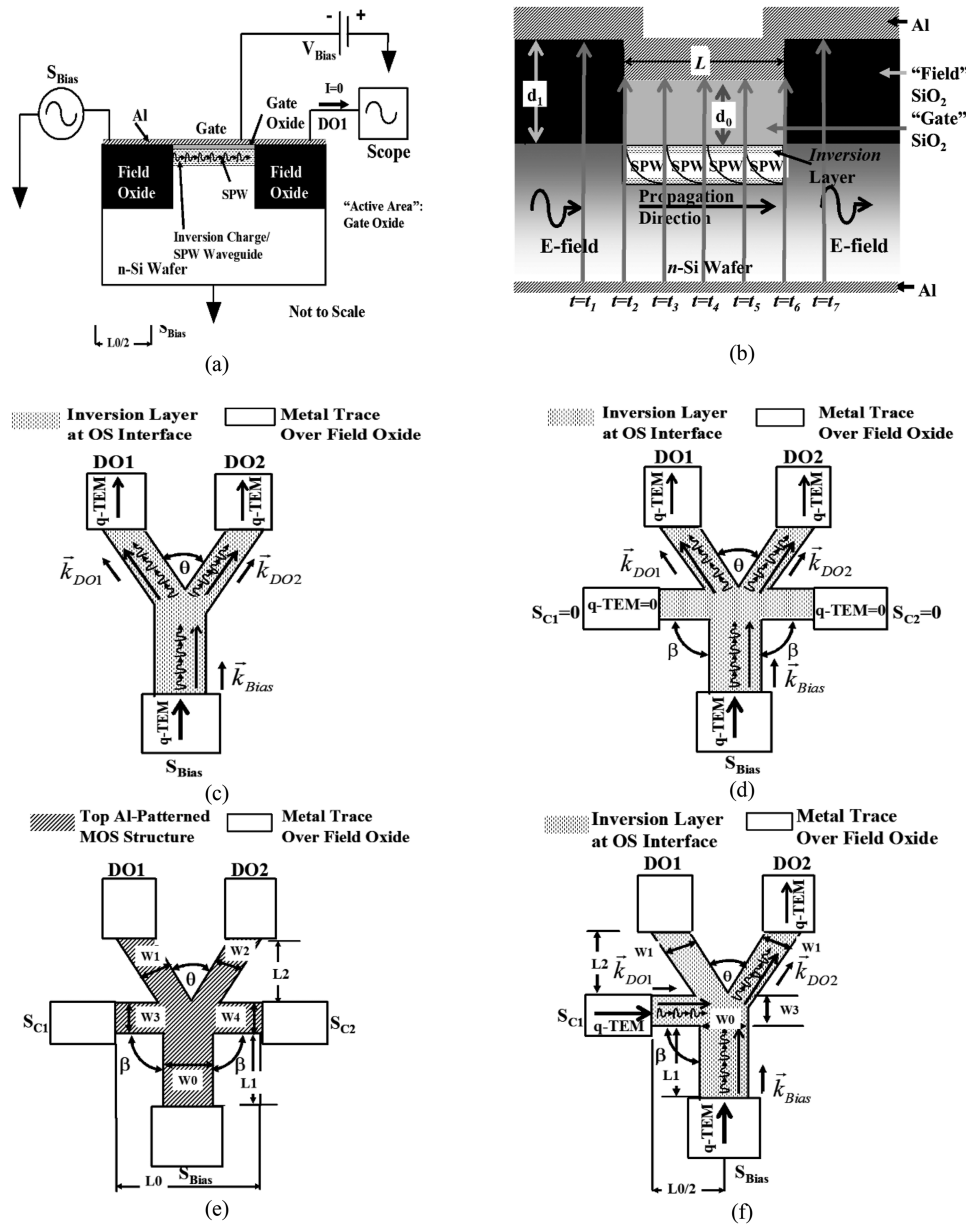


FIG. 1. Conceptual development of PPL and visualization of SPW launch, propagation, interaction, and detection. (a) MOS biased by V_{Bias} ; signal at DO1 is measured with high-impedance probe ($I = 0$). (b) Cross section of (a); d_0 and d_1 are gate and field oxide thicknesses, respectively, and L is the channel length. $t_1, \dots, t_7$ represent snapshots in time at which SPWs are regenerated; in reality, $\Delta t \approx 0$. (c) MOS patterned as "Y" with angle θ between outputs. (d) MOS in (c) with added lateral channels at angles β , but having no signals S_{C1} and S_{C2} impinging upon them. (e) Sketch of full PPL device.^{13,14} (f) Sketch of partial PPL. Straight and wiggly arrows represent q-TEM waves and SPWs, respectively.

be localized/damped (short-range).¹⁶ However, such a charge disturbance keeps being regenerated continually at the front-end of the q-TEM wave as it propagates toward DO1. We refer to the charge disturbance as a generated localized surface plasma wave (SPW). Because the SPW is generated/transported coincident with the q-TEM's front-end, its dispersion relation (and speed) is that

of the latter. Due to its localized nature, the traditional coherent spatial oscillation of the whole inversion layer charge density does not occur, and there is no necessity to define an SPW oscillation frequency.¹⁷ The continual regeneration of SPWs by the q-TEM wave essentially precludes/avoids their damping^{18,19} until DO1 is reached where the combination q-TEM/SPW is detected as a volt-

age [Fig. 1(a)]. After V_{Bias} is so large that the electron density in the inversion layer reaches saturation, there are no other possible sources of nonlinearity; the device is linear. Therefore, the input and output waveforms should look similar.

Second, if instead of a straight channel, we pattern the “Y” MOS structure [Fig. 1(c)] and bias it into inversion, the propagating “Bias” q-TEM/SPWs generated by the signal S_{Bias} would split upon reaching the junction (due to symmetry) and continue to propagate toward DO1 and DO2, where they are detected as substantially equal voltages. In the absence of MOS inversion (or accumulation), i.e., at $V_{\text{Bias}} = 0$, only the q-TEM wave would be propagating and split at the junction and be detected at DO1 and DO2. The detected voltage in the presence of SPWs would be different than in their absence; this behavior is experimentally demonstrated below.

An antecedent to the PPL device, which embodies the “Y” structure, but with lateral channels (to be explained shortly) converging at the junction, into which no q-TEM waves impinge, is shown in Fig. 1(d). This structure is symmetrical with respect to the junction and behaves similar to that in Fig. 1(c).

Third, the MOS structure in Fig. 1(e), while identical to that in Fig. 1(d), becomes asymmetric when a signal is applied at either S_{C1} (with $S_{C2} = 0$) or S_{C2} (with $S_{C1} = 0$). In the former case, the repulsive interaction of the q-TEM/SPWs generated by S_{C1} and the “Bias” q-TEM/SPWs near the junction causes the latter to be steered toward DO2. For a signal in S_{C2} (with $S_{C1} = 0$), the “Bias” q-TEM/SPWs are steered toward DO1. This is the rather timely unorthodox PPL device, whose performance was previously theoretically projected to exhibit femtojoule power dissipations and femtoseconds switching speeds.¹³ PPL represents a departure from cost-prohibitive nanoscale CMOS computing, yet as a universal digital logic gate, it is poised to meet the demanding performance needs of emerging computing systems, such as Central Processing Units (CPUs), graphic CPUs, and Artificial Intelligence Processing Units (AI PUs).^{20–22}

Since PPL relies on the interaction of only two q-TEM/SPWs at a time, to demonstrate its key aspects of regenerative transport, repulsive SPW–SPW switching/steering, and detection, it is only necessary to study the partial PPL [Fig. 1(f)]. We briefly present the fundamentals of the partial-PPL device design procedure, which is given in detail elsewhere.¹³

The partial-PPL derives conceptually from the differential scattering cross section for quantum particles in momentum states p_1 and p_2 , experiencing a scattering event into the solid angle (θ, ϕ) , and transitioning to output states p_3 and p_4 [Fig. 2].¹³ In particular, for plasmon–plasmon scattering, A_{fi} is given by

$$A_{fi} = 4 \left(\frac{\pi^2 e^2}{m^* \omega_0} \right)^2 \cos \theta_{k_{\text{Bias}} k_{C1}} \cos \theta_{k_{\text{DO1}} k_{\text{DO2}}} \pi_0(k_{\text{Bias}} + k_{C1}), \quad (1)$$

where

$$\pi_0(k) = \int \frac{d^3 p}{(2\pi)^3} G_0(p+k) G_0(p), \quad (2)$$

with G_0 being the single-particle free propagator Green’s function. The kinematics of the general scattering process [Fig. 2(a)] may be mapped into the partial-PPL structure [Fig. 1(f)]. The square of the charge in (1) signals the presence of the Coulomb force in the

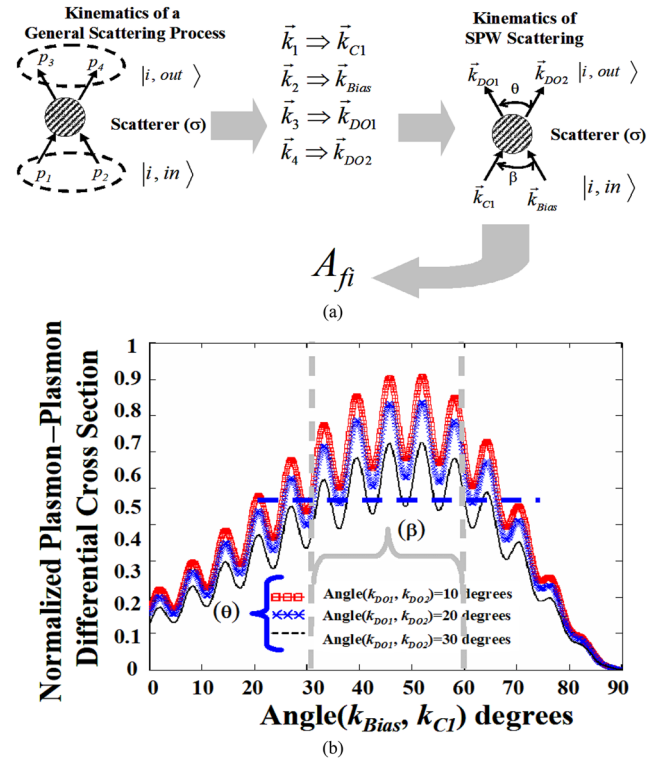


FIG. 2. Partial-PPL design principles. (a) Kinematics of scatterer with cross section σ for general and partial-PPL cases, leading to the Feynman amplitude A_{fi} determining $d\sigma/d\theta$,¹³ the differential scattering cross section (DSCS).¹³ (b) Determination of device angles. The plot shows the normalized DSCS for various incoming angles β and detector angles θ . Assumptions: in the coordinate system employed, the momenta are defined as follows: $\vec{p} = |\vec{p}| \cdot \hat{j}$, $\vec{k}_{\text{Bias}} = |\vec{k}_{\text{Bias}}| \cdot \hat{j}$, $\vec{k}_{C1} = -|\vec{k}_{C1}| \cos(\theta_{k_{\text{Bias}} k_{C1}}) \cdot \hat{j} + |\vec{k}_{C1}| \sin(\theta_{k_{\text{Bias}} k_{C1}}) \cdot \hat{j}$, $|\vec{k}_{\text{Bias}}| = |\vec{k}_{C1}| = 0.5k_F$, $|k_F| = \sqrt{2\pi n_s}$, $m^* = 1.08m_0$, $\omega = \omega_0 = 7.022 \times 10^{13} \text{ s}^{-1}$, $n_s = 6.295 \times 10^{16} \text{ m}^{-2}$, $\epsilon_r = 11.8$, and $T = 300 \text{ K}$. The integration limits over p are $0.01k_F$ and k_F .¹³

interaction. Once the propagation of the “Bias” and “Control” q-TEM/SPWs with respective momenta $\vec{k}_{\text{Bias}}$ and $\vec{k}_{C1}$ is established, their interaction at the junction results in deflection into the desired output DO2, as dictated by momentum conservation law, $\vec{k}_{\text{Bias}} + \vec{k}_{C1} = \vec{k}_{\text{DO2}}$.¹³

We conducted two experiments, measuring an implementation of Fig. 1(d), with $\theta = 10^\circ$ and $\beta = 30^\circ$ (see Fig. 3), and an implementation of Fig. 1(f), with $\theta = 30^\circ$ and $\beta = 60^\circ$ (see Fig. 4). Both cases assumed the set of material properties in Fig. 2. The remaining parameters, namely, the quasi-TEM/SPW waveguide widths, lengths, and junction dimensions, were then determined. Since PPL relies on wave guiding on MOS microstrip lines,²³ techniques to minimize reflection, e.g., impedance matching and waveguide tapering,²⁴ were invoked; the lengths L0, L1, and L2 were chosen much larger than the SPWs’ damping length. Both devices have their aluminum (Al) gate biased by “ V_{Bias} ,” which is swept between -30 V and $+30 \text{ V}$, including $V_{\text{Bias}} = 0$. The devices consist of an n-type silicon MOS structure with patterned Al gate over a $400 \text{ \AA}$ -thick SiO_2

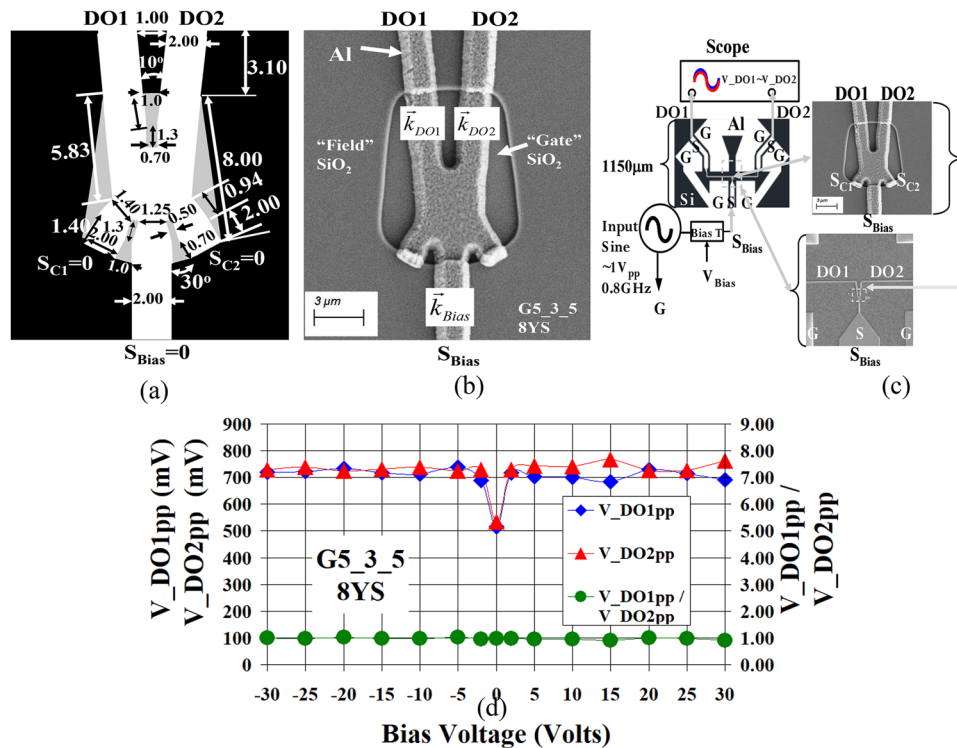


FIG. 3. Measurement of symmetric device (with $S_{C1} = S_{C2} = 0$) sketched in Fig. 1(d). (a) Layout (in μm) and (b) Scanning Electron Micrograph (SEM) of device. Input q-TEM/SPWs propagate in direction $\vec{k}_{Bias}$, and the outputs propagate in directions $\vec{k}_{DO1}$ and $\vec{k}_{DO2}$. (c) Coplanar-waveguide (ground-signal-ground) test setup: the signal “ S_{Bias} ” propagates to junction, and the outputs at DO1 and DO2 are measured. (d) Measured peak-to-peak amplitudes at DO1 and DO2 as V_{Bias} is swept from -30 to 30 V. Legends: triangles and diamonds: left vertical axis; circles: right vertical axis.

dielectric. Capacitance-voltage measurements on these MOS structures showed that at $V_{Bias} = 0$ V, they are neither in inversion nor in accumulation,¹⁵ but that at $V_{Bias} = -10$ V and $+10$ V, they are in inversion and accumulation, respectively. Outside the MOS area, the Al tops a 4300 Å-thick “field” oxide. Measurement results at 294 K and a brief discussion is given below.

Figure 3 shows an implementation of the symmetric structure [Fig. 1(d)] and plots of V_{DO1pp} and V_{DO2pp} . At $V_{Bias} = 0$ V, the input q-TEM wave (S_{Bias}) propagates²⁴ yielding output voltages $V_{DO1pp} = 516.3$ mV and $V_{DO2pp} = 533.5$ mV, i.e., within 3%; this difference is attributed to fabrication-derived asymmetry. When under inversion, the structure yields output voltages $V_{DO1pp} = 713.4$ V and $V_{DO2pp} = 737.4$ V, also within 3% of each other, but at an average of 39% higher than those at $V_{Bias} = 0$ V. These greater output voltages verify that under inversion, there is an extra entity present in addition to the propagating q-TEM wave, accompanying it, that is, what we have described earlier as SPWs, which are responsible for the larger detected voltages at $V_{Bias} = -10$ V vs at $V_{Bias} = 0$ V.

Figure 4 shows an implementation of the partial PPL [Fig. 1(f)] and plots of V_{DO1pp} and V_{DO2pp} . At $V_{Bias} = 0$ V, the input q-TEM waves (S_{Bias} and S_{C1}) propagate to converge at and emerge from the junction (like in a four-port/-terminal microstrip junction)²⁴ and arrive at DO1 and DO2 yielding output voltages $V_{DO1pp} = 254$ mV and $V_{DO2pp} = 249$ mV, i.e., within 2%;

this is attributed to fabrication-derived asymmetry. For the structure under inversion, the q-TEM waves (S_{Bias} and S_{C1}) generate and transport SPWs at their front-end, so the combined q-TEM/SPWs with momenta $\vec{k}_{Bias}$ and $\vec{k}_{C1}$ interact (as conceived) repulsively at the junction, yielding the detected voltage $V_{DO2pp} = 320$ mV. A voltage $V_{DO1pp} = 226$ mV is also detected. This cannot be attributed to fabrication-derived asymmetry, however, since the difference due to asymmetry can only be 2%, whereas the difference between V_{DO1pp} and V_{DO2pp} is 41%. This difference must be due to the SPW-SPW repulsive interaction, the effect we sought to demonstrate. Ideally, V_{DO1pp} should be zero; however, a leakage of the “ S_{Bias} ” q-TEM/SPWs into the $\vec{k}_{DO1}$ direction occurs due to, for example, a difference in arrival time at the junction of the $\vec{k}_{Bias}$ and $\vec{k}_{C1}$ q-TEM/SPWs, which allows the “Bias” q-TEM/SPWs to partially escape/miss the repulsive influence from the S_{C1} q-TEM/SPWs. The scattering “efficiency” of the process into $\vec{k}_{DO2}$ may be improved by achieving equal-length microstrip lines S_{Bias} and S_{C1} from the outputs of the Bias-T to the device active area; bending the S_{Bias} line near the active region by 90° was aimed at doing that [see Figs. 4(b) and 4(c)]. Further optimization may include engineering the shape of the S_{Bias} and S_{C1} waveforms to maximize SPW-SPW interaction time at the junction.

In conclusion, the repulsive interaction of quasi-TEM wave-transported “localized” SPWs at room temperature in the inversion

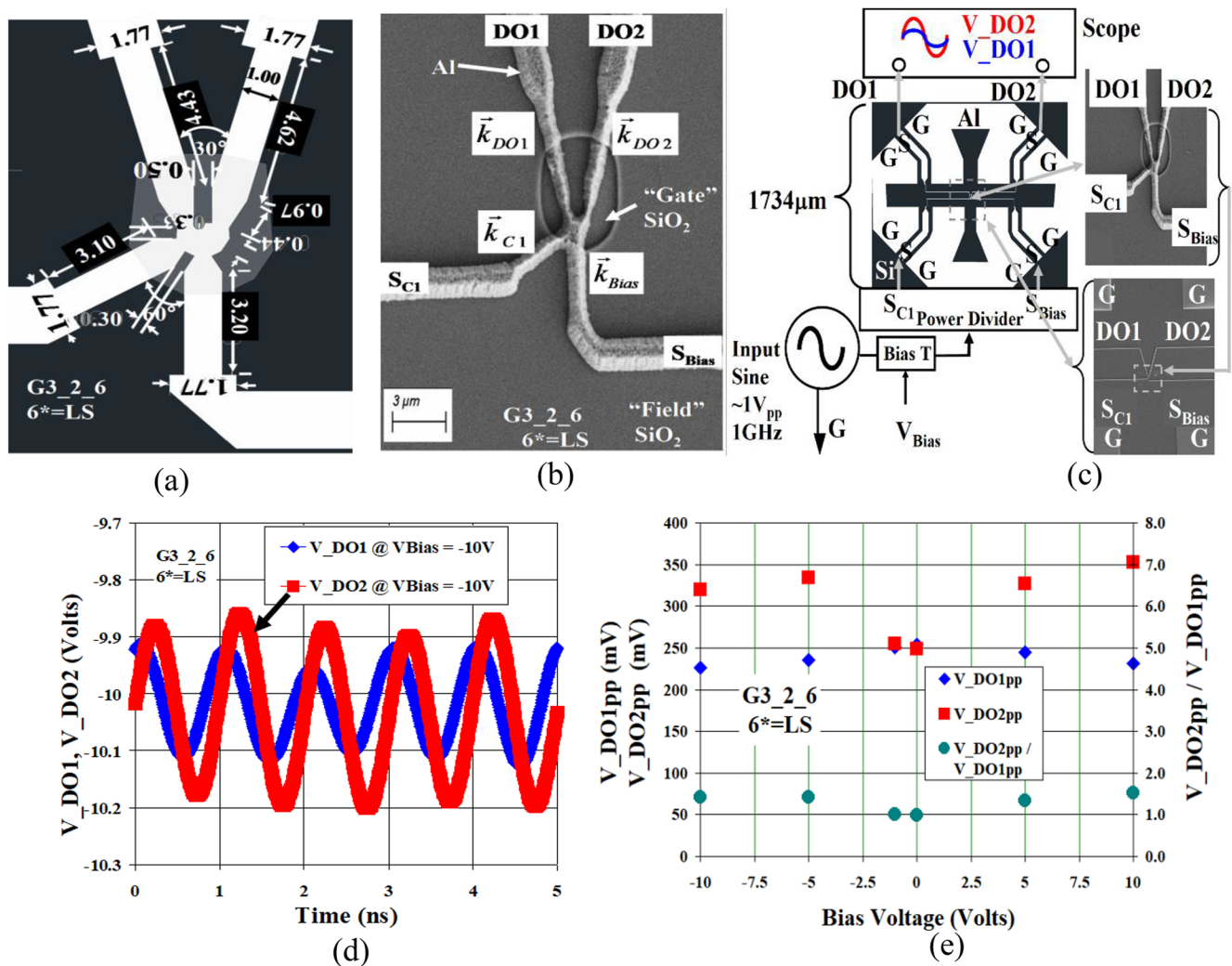


FIG. 4. Partial PPL, test setup, and measurement results. (a) Layout (in μm) and (b) SEM of device. Input q-TEM/SPWs in directions k_{Bias} and k_{C1} propagate toward junction, interact repulsively (for $V_{Bias} \neq 0$ V), and emerge in direction k_{DO2} , due to a difference in, for example, arrival time at junction; a leakage component escapes into direction k_{DO1} . (c) Coplanar-waveguide (ground–signal–Ground) test setup: equal-amplitude signals S_{Bias} and S_{C1} propagate to junction, and outputs at DO1 and DO2 are measured. (d) DO1 and DO2 waveforms. (e) V_{DO1pp} and V_{DO2pp} vs V_{Bias} . Legends: squares and diamonds: left vertical axis; triangles: right vertical axis.

layer of a patterned MOS structure was observed. This fundamental result paves the way for the development of plasmon–plasmon scattering logic (PPL), a revolutionary digital logic concept based on the generation, propagation, and manipulation of plasmons in an electron fluid (EF), which was previously theoretically projected to exhibit femtojoule power dissipations and femtosecond switching speeds, while not demanding expensive nanometer-scale silicon (Si) technology fabrication processes for its implementation.

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AUTHOR DECLARATIONS

Conflict of Interest

H.J.D.L.S. has Patent 8,509,584 related to this work issued.

Author Contributions

H. J. De Los Santos: Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal). **J. Ge:** Methodology (equal); Validation (equal). **G. Wang:** Data curation (equal); Methodology (equal); Supervision (equal); Writing – review & editing (equal). **S. Ding:** Data curation (equal); Methodology (equal). **P. R. Berger:** Methodology (equal);

Writing – review & editing (equal). **D. R. Gajula:** Investigation (equal); Methodology (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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